UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,068	05/01/2001	Yoav Almog	42390P10913	6986

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EXAMINER
HUISMAN, DAVID J

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<table>
<tr><td rowspan="3">Office Action Summary</td><td colspan="2">Application No.</td><td colspan="2">Applicant(s)</td></tr>
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<tr><td>Examiner</td><td>Art Unit</td><td></td></tr>
<tr><td></td><td>David J. Huisman</td><td>2183</td><td></td></tr>
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-- The MAILING DATE of this communication appears on th cover sheet with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _29 November 2004_.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-22_ is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-22_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on _01 May 2001_ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a) ☐ All   b) ☐ Some * c) ☐ None of:

   1. ☐ Certified copies of the priority documents have been received.

   2. ☐ Certified copies of the priority documents have been received in Application No. _____.

   3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-22 have been examined.

Papers Submitted

2.   It is hereby acknowledged that the following papers have been received and placed of

record in the file: RCE and Amendment as received on 11/29/2004.

Withdrawn Rejections

3.   Applicant has overcome the prior art rejections set forth in the previous Office Action.

Consequently, these rejections have been withdrawn by the examiner, thereby rendering

applicant's arguments moot. However, upon further consideration, a new ground(s) of rejection

are applied below.

Claim Objections

4.   Claim 1 is objected to because of the following informalities: Applicant states "first

occurrence" twice in a row in the last two lines of the claim, and the examiner feels that this may

be a typo. If so, please correct this portion of the claim. Appropriate correction is required.

5.   Claim 20 is objected to because of the following informalities: The examiner feels that

the word "calculated" is in an inappropriate position. Please reword this claim. Appropriate

correction is required.

6.   Claim 21 is objected to because of the following informalities: The examiner feels that the word "predicted" is in an inappropriate position. Please reword this claim. Appropriate correction is required.

7.   Claim 22 is objected to because of the following informalities: The examiner feels that the word "predicted" is in an inappropriate position. Please reword this claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9.   Claims 20-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10.   Claims 20-22 recite the limitation "the first target". There is insufficient antecedent basis for this limitation in the claim.

11.   Also, it is not clear what applicant is trying to claim in claims 20-22, as the language makes very little sense to the examiner. It is asked that applicant reword the claim. For purposes of this examination, the examiner is interpreting each of these claims as claiming that the target of the first occurrence of the branch instruction and the target of the re-encountered branch instruction are the same.

Claim Rejections - 35 USC § 102

12.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13.   Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Lempel, U.S.

Patent No. 5,978,909.

14.   Referring to claim 1, Lempel has taught a method comprising:

a) calculating a target of a first occurrence of a branch instruction using a decoder. See column

5, line 65, to column 6, line 3. Basically, the first time a branch is encountered, a static predictor,

which is part of the decoder (column 3, lines 54-55), calculates the target address (column 11,

line 27).

b) storing the target of the first occurrence of the branch instruction before the first occurrence of

the branch instruction is fully executed. See column 5, line 65, to column 6, line 9. Note that

when a static prediction occurs, an entry is allocated in the speculative BTB 150 (Fig.1 - SBTB),

and this entry includes the calculated target address (Fig.3c, component 312). -

c) re-encountering the branch instruction before the first occurrence of the branch instruction is

fully executed. See column 6, lines 3-10.

d) calculating a target for the re-encountered branch instruction by accessing the target stored

prior to determining a target for the re-encountered branch instruction using the decoder and

before the first occurrence of the first occurrence of the branch instruction is fully executed. See

column 6, lines 3-8, and column 12, line 41, to column 13, line 9.

15.   Referring to claim 2, Lempel has taught a method as described in claim 1. Lempel has

further taught that the branch instruction is a direct branch. See column 11, lines 27-29, and note

that an action is performed for all branches except for indirect branches (i.e., direct branches).

16.   Referring to claim 3, Lempel has taught a method as described in claim 1. Lempel has

further taught that the branch instruction is a backward branch. See column 2, lines 18-19.

17.   Referring to claim 4, Lempel has taught a method as described in claim 1. Lempel has

further taught that storing the target of the first occurrence comprises saving the target to a cache.

As described in column 6, line 3, the target address is stored in an entry in the SBTB (Fig.3C).

The SBTB, as disclosed by Lempel in column 4, lines 63-65, is in fact a cache. Therefore, the

target is saved to a cache.

18.   Referring to claim 5, Lempel has taught a method as described in claim 4. Lempel has

further taught that the target of the first occurrence of the branch instruction is also stored in a

branch prediction unit after the first occurrence of the branch instruction has been fully executed.

See column 6, lines 5-8.

19.   Referring to claim 6, Lempel has taught a method as described in claim 5. Lempel has

further taught that the target for the re-encountered branch instruction is calculated before the

target of the first occurrence of the branch instruction is stored in the branch prediction unit. See

column 6, lines 3-10, and column 12, line 41, to column 13, line 9.

20.   Referring to claim 7, Lempel has taught a method as described in claim 6. Lempel has

further taught that calculating a target for the re-encountered branch instruction comprises

accessing at least one target stored in at least one of the cache and the branch prediction unit,

prioritizing the accessed targets, and generating a branch prediction based on the prioritized

targets. See Fig.2 and note that the branch prediction (predicted Target IP) is generated via

selector 170. Selector 170 selects one of either the predicted target from the cache 150 or the

predicted target from the prediction unit 145. The selection is based on if there is a valid hit in

the prediction unit, and therefore, the prediction unit's target is given priority. See column 6,

lines 49-64 for more of an explanation.

21.   Referring to claim 8, Lempel has taught an apparatus comprising:

a) a decoder to calculate a target of a first occurrence of a branch instruction. See column 5, line

65, to column 6, line 3. Basically, the first time a branch is encountered, a static predictor, which

is part of the decoder (column 3, lines 54-55), calculates the target address (column 11, line 27).

b) a cache to store the target of the first occurrence of the branch instruction before the first

occurrence of the branch instruction is fully executed. See column 5, line 65, to column 6, line

9. Note that when a static prediction occurs, an entry is allocated in the SBTB 150 (Fig.1), and

the target address is store in this entry (Fig.3c, component 312). The SBTB, as disclosed by

Lempel in column 4, lines 63-65, is in fact a cache. Therefore, the target is saved to a cache.

c) a branch prediction unit to, upon re-encountering the branch instruction before the first

occurrence of the branch instruction is fully executed, predict a target of the re-encountered

branch instruction by accessing the target of the first occurrence of the branch instruction stored

in the cache prior to determining a target for the re-encountered branch instruction using the

decoder and before the first occurrence of the branch instruction is fully executed. See column 6,

lines 3-10, and column 12, line 41, to column 13, line 9.

22.   Referring to claim 9, Lempel has taught an apparatus as described in claim 8.

Furthermore, the method of claim 2 is performed by the apparatus of claim 9. Therefore, claim 9

is rejected for the same reasons set forth in the rejection of claim 2.

23.   Referring to claim 10, Lempel has taught an apparatus as described in claim 8.

Furthermore, the method of claim 3 is performed by the apparatus of claim 10. Therefore, claim

10 is rejected for the same reasons set forth in the rejection of claim 3.

24.   Referring to claim 11, Lempel has taught an apparatus as described in claim 8.

Furthermore, the method of claim 5 is performed by the apparatus of claim 11. Therefore, claim

11 is rejected for the same reasons set forth in the rejection of claim 5.

25.   Referring to claim 12, Lempel has taught an apparatus as described in claim 11.

Furthermore, the method of claim 6 is performed by the apparatus of claim 12. Therefore, claim

12 is rejected for the same reasons set forth in the rejection of claim 6.

26.   Referring to claim 13, Lempel has taught an apparatus as described in claim 12.

Furthermore, the method of claim 7 is performed by the apparatus of claim 13. Therefore, claim

13 is rejected for the same reasons set forth in the rejection of claim 7.

27.   Referring to claim 14, Lempel has taught a system comprising:

a) a processor capable of pipelining instructions. See column 12, lines 13-14.

b) a decoder to calculate a target of a first occurrence of a branch instruction to be executed by

the processor. See column 5, line 65, to column 6, line 3. Basically, the first time a branch is

encountered, a static predictor, which is part of the decoder (column 3, lines 54-55), calculates

the target address (column 11, line 27).

c) a cache to store the target of the first occurrence of the branch instruction before the first

occurrence of the branch instruction is fully executed by the processor. See column 5, line 65, to

column 6, line 9. Note that when a static prediction occurs, an entry is allocated in the SBTB

150 (Fig.1), and the target address is store in this entry (Fig.3c, component 312). The SBTB, as

disclosed by Lempel in column 4, lines 63-65, is in fact a cache. Therefore, the target is saved to

a cache.

d) a branch prediction unit to, upon re-encountering the branch instruction before the first

occurrence of the branch instruction is fully executed, predict a target of the re-encountered

branch instruction by accessing the target of the first occurrence of the branch instruction stored

in the cache prior to determining a target for the re-encountered branch instruction using the

decoder and before the first occurrence of the branch instruction is fully executed. See column 6,

lines 3-10, and column 12, line 41, to column 13, line 9.

28.   Referring to claim 15, Lempel has taught a system as described in claim 14.

Furthermore, claim 15 is rejected for the same reasons set forth in the rejection of claim 9.

29.   Referring to claim 16, Lempel has taught a system as described in claim 14.

Furthermore, claim 16 is rejected for the same reasons set forth in the rejection of claim 10.

30.   Referring to claim 17, Lempel has taught an apparatus as described in claim 14.

Furthermore, claim 17 is rejected for the same reasons set forth in the rejection of claim 11.

31.   Referring to claim 18, Lempel has taught an apparatus as described in claim 17.

Furthermore, claim 18 is rejected for the same reasons set forth in the rejection of claim 12.

32.   Referring to claim 19, Lempel has taught an apparatus as described in claim 18.

Furthermore, claim 19 is rejected for the same reasons set forth in the rejection of claim 13.

33.   Referring to claim 20, Lempel has taught a method as described in claim 1. Lempel has

further taught that the target of the first occurrence of the branch instruction, the target of the re-

encountered branch instruction calculated, and the first target are the target of the re-encountered

branch instruction determined are the same target. See column 12, lines 41-59, and note that the

same backward branch is predicted to be taken and the targets are the same as the system

branches back to the beginning of the loop.

34.   Referring to claim 21, Lempel has taught an apparatus as described in claim 8.

Furthermore, the method of claim 20 is performed by the apparatus of claim 21. Therefore,

claim 21 is rejected for the same reasons set forth in the rejection of claim 20.

35.   Referring to claim 22, Lempel has taught an apparatus as described in claim 14.

Furthermore, claim 22 is rejected for the same reasons set forth in the rejection of claim 21.

Conclusion

36.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure. Applicant is reminded that in amending in response to a rejection of claims, the

patentable novelty must be clearly shown in view of the state of the art disclosed by the

references cited and the objections made. Applicant must also show how the amendments avoid

such references and objections. See 37 CFR § 1.111(c).

Intel Corporation, WO 94/27210, has taught a speculative history mechanism in a branch

target buffer.

Kitta, U.S. Patent No. 5,394,530, has taught an arrangement for predicting a branch target

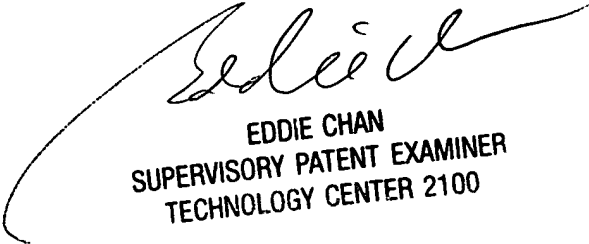address in the second iteration of a short loop.

Col et al., U.S. Patent No. 6,526,502, has taught an apparatus and method for

speculatively updating global branch history with branch prediction prior to resolution of branch

outcome.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168.

The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
January 12, 2004

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SUPERVISORY PATENT EXAMINER
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